Cell Processor and Playstation 3

Guillem Borrell i Nogueras

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- Cell systems
- Bad news
- More bad news

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- Good news
- Q&A

IBM Blades

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QS21

- Cell BE based.
- 460 Gflops Float
- 20 GFLops Double
- QS22
 - PowerXCell 8i based
 - 460 GFlops Float
 - 200 GFlops Double

IBM Blades

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QS21

- Cell BE based.
- 460 Gflops Float
- 20 GFLops Double
- QS22
 - PowerXCell 8i based
 - 460 GFlops Float
 - 200 GFlops Double
 - No SPU Double precision improvements expected from IBM

Playstation 3

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- Cell BE based.
- 460 Gflops Float
- 20 GFLops Double

Playstation 3

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- Cell BE based.
- 460 Gflops Float
- 20 GFLops Double
- 256 MB RAM

IBM Power 7

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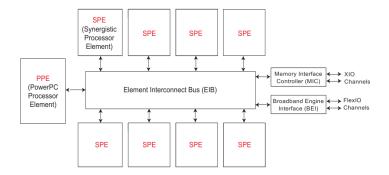
- 8 cores
- 4 threads per core (32 Threads!)
- ? SPE

IBM Power 7

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- 8 cores
- 4 threads per core (32 Threads!)
- ? SPE
- 1 TFlop on a chip

Cell Broadband Engine



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¿How does it compute?

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- PPU starts a program
- PPU loads an SPU context on a thread
- SPU context loads all necessary data into its LS
- SPU executes context
- SPU ends the task and returns control to PPU



Synergistic Processor Element (SPE)
Synergistic Processor Unit (SPU)
Local Store (LS)
Memory Flow Controller (MFC)
DMA Controller

PPE PowerPC Processor Element

- PPU PowerPC Processor Unit
 - **EIB** Element Interconnect Bus
- SPE Synergistic Processor Element
- SPU Synergistic Processor Unit
- MFC Memory Flow Controller
- DMA Direct Memory Access
- SIMD Single Instruction Multiple Data

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Dumb vector unit

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- General purpose vector unit
 - Designed to run code
 - Altivec unit on a box
 - IBM called that VMX

Dumb vector unit

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 - No type distinction
 - Data should be aligned by hand

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- General purpose vector unit
 - Designed to run code
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- LS is regiser based
 - No type distinction
 - Data should be aligned by hand
- MFC is a DMA controller
 - Data moved with DMA primitives.
 - No data scheduling
 - No data implicit copying.

SIMD Programming

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- SPUs are programmed using SIMD primitives
- Like a vector unit

SIMD Programming

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- SPUs are programmed using SIMD primitives
- Like a vector unit
- Almost coding in assembly
 - Access assembly instructions via libspu2
 - Add to that DMA instructions

SIMD Programming

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- SPUs are programmed using SIMD primitives
- Like a vector unit
- Almost coding in assembly
 - Access assembly instructions via libspu2
 - Add to that DMA instructions
 - That can take us ages

PPU and SPU code

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- PPE have L1 and L2 cache.
- SPE have LS (register based)

PPU and SPU code

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- PPE have L1 and L2 cache.
- SPE have LS (register based)
- Their ssembly has nothing to do
 - They are compiled separately.
 - PPU code cannot be reused.

PPU code libraries

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- BLAS (Basic Linear Algebra Subroutines)
- LAPACK (Linear Algebra Package)
- FFTW (The Fastest Fourier Transform in the West)
- C and Fortran interfaces
- Fortran interface is not complete

PPU code libraries

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- BLAS (Basic Linear Algebra Subroutines)
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- FFTW (The Fastest Fourier Transform in the West)
- C and Fortran interfaces
- Fortran interface is not complete
- Almost all we need is in Cell SDK!

Thin ice

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- PPU code means no SPU control.
- Data must be aligned too using posix_memalign.
- If SPU control is needed PPU code cannot be used at all
- Tells us what we can or cannot do
- BSC has been using those for about 2 years.

Optimizing compilers

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- Cell Superscalar
 - Alpha state
 - OpenMP-like annotations
 - BSC
 - Free Software
- XL compilers for Multicore Acceleration
 - Alpha state
 - OpenMP support
 - MASS (Mathematical Acceleration Subsystem)
 - Worth the money

Conclusions

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• PPU code is possible

Conclusions

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- PPU code is possible
- SPU code is not possible for us
- 2 options:
 - Cell SDK for Multicode Acceleration
 - Optimizing Compiler (WAIT)

Conclusions

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- PPU code is possible
- SPU code is not possible for us
- 2 options:
 - Cell SDK for Multicode Acceleration
 - Optimizing Compiler (WAIT)
- Get a good C book.

Q&A

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